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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/500,065 | 06/24/2004 | Hiroshi Miyagi | TIC-0067 | 5575 |

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| EXAMINER | |
|---|---|
| NGUYEN, TUAN HOANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2643 | |

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/500,065 | MIYAGI, HIROSHI | |
| | Examiner | Art Unit | |
| | Tuan H. Nguyen | 2643 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/11/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## *DETAILED ACTION*

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) submitted on 08/11/2004 has been considered by Examiner and made of record in the application file.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al. (US PAT. 5,140,704 hereinafter, "Ueno") in view of Toda et al. (U.S

PAT. 6,061,279 hereinafter, "Toda").

Regarding claim 1, Ueno discloses a noise removing circuit, comprising: a highpass filter detecting a noise component included in an input signal (Fig. 1 col. 1 lines 18-21); a pulse generating circuit generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said highpass filter becomes a predetermined reference voltage or higher (Fig. 1 col. 1 lines 12-31); an analog delaying circuit delaying the input signal by a predetermined amount of time, and outputting the delayed signal (Fig. 1 col. 1 lines 12-16); and an outputting circuit holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse generated by said pulse generating circuit is input, and outputting the signal output from said analog delaying circuit unchanged in other cases (Fig. 1 col. 1 lines 12-31). Ueno differs from the claimed invention in not specifically teaching analog delaying circuit comprises a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to the plurality of capacitors in a predetermined order at different timing, and a plurality of second switches extracting the voltage of the input signal respectively held by said plurality of capacitors before next timing when the voltage is held is reached. However, Toda teaches an analog delaying circuit comprises a plurality of capacitors (Fig. 2 col. 6 lines 31-47), a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the

input signal to the plurality of capacitors in a predetermined order at different timing (Fig. 2 col. 1 lines 11-31), and a plurality of second switches extracting the voltage of the input signal respectively held by said plurality of capacitors before next timing when the voltage is held is reached (Fig. 2 col. 1 lines 11-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ueno for analog delaying circuit comprises a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to the plurality of capacitors in a predetermined order at different timing, and a plurality of second switches extracting the voltage of the input signal respectively held by said plurality of capacitors before next timing when the voltage is held is reached as per teaching of Toda, because it provides a delay circuit for analog signals, which is capable of eliminating the influence of noise of low frequency as disturbance.

Regarding claim 2, Ueno discloses a noise removing circuit, comprising: a noise extracting circuit extracting a noise component included in an input signal (Fig. 1 col. 1 lines 18-21); a pulse generating circuit generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said noise extracting circuit becomes a predetermined reference voltage or higher (Fig. 1 col. 1 lines 12-31); and an outputting circuit holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse having the predetermined width is output from said pulse generating circuit, and outputting the signal output from said analog

delaying circuit unchanged in other cases (Fig. 1 col. 1 lines 12-31). Ueno differs from the claimed invention in not specifically teaching an analog delaying circuit having a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing, and a plurality of second switches making said plurality of capacitors output the voltage of the input signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit. However, Toda teaches an analog delaying circuit having a plurality of capacitors (Fig. 2 col. 6 lines 31-47), a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing (Fig. 2 col. 1 lines 11-31), and a plurality of second switches making said plurality of capacitors output the voltage of the input signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit (Fig. 2 col. 1 lines 11-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ueno for analog delaying circuit comprises a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by

respectively supplying the input signal to the plurality of capacitors in a predetermined order at different timing, and a plurality of second switches extracting the voltage of the input signal respectively held by said plurality of capacitors before next timing when the voltage is held is reached as per teaching of Toda, because it provides a delay circuit for analog signals, which is capable of eliminating the influence of noise of low frequency as disturbance.

Regarding claim 3, Ueno discloses a noise removing circuit, comprising: a noise extracting circuit extracting a noise component included in an input signal (Fig. 1 col. 1 lines 18-21); a pulse generating circuit generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said noise extracting circuit becomes a predetermined reference voltage or higher (Fig. 1 col. 1 lines 12-31); and an outputting circuit holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse having the predetermined width is output from said pulse generating circuit, and outputting the signal output from said analog delaying circuit unchanged in other cases, wherein all of said circuits are formed on a same semiconductor substrate with a MOS process (Fig. 1 col. 1 lines 12-31). Ueno differs from the claimed invention in not specifically teaching an analog delaying circuit having a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing, and a plurality of second switches making said

plurality of capacitors output the voltage of the input signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit. However, Toda teaches an analog delaying circuit having a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing (Fig. 2 col. 1 lines 11-31), and a plurality of second switches making said plurality of capacitors output the voltage of the input signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit (Fig. 2 col. 1 lines 11-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ueno for an analog delaying circuit having a plurality of capacitors, a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing, and a plurality of second switches making said plurality of capacitors output the voltage of the input signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit as per teaching of Toda, because it provides a delay circuit for

analog signals, which is capable of eliminating the influence of noise of low frequency as disturbance.

Regarding claim 4, Toda further discloses output terminals of said plurality of second switches are connected in common (Fig. 1 col. 1 lines 20-31).

Regarding claim 5, Toda further discloses plurality of first switches are exclusively made electrically continuous (Fig. 1 col. 1 lines 32-42).

Regarding claim 6, Toda further discloses plurality of second switches are exclusively made electrically continuous (Fig. 1 col. 1 lines 32-42).

Regarding claim 7, Toda further discloses each of said pluralities of first and second switches is an analog switch configured by connecting an FET of a p-channel type, and an FET of an n-channel type in parallel (Fig. 9 col. 16 lines 35-44).

Regarding claim 8, Toda further discloses analog delaying circuit further comprises clock generating means for generating a clock signal that cyclically selects each of said plurality of first switches and said plurality of second switches (Fig. 9 col. 7 lines 19-45).

Regarding claim 9, Toda further discloses clock generating means supplies a clock signal, whose one cycle is an amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit, to said plurality of first switches and said plurality of second switches in a sequential order (col. 7 lines 33-45).

Regarding claim 10, Toda further discloses analog delaying circuit further comprises an output capacitor connected to each of said plurality of capacitors via said plurality of second switches (Fig. 2 col. 6 lines 31-47).

Regarding claim 11, Toda further discloses a capacitance of said output capacitor is set to a value smaller than a capacitance of each of said plurality of capacitors (col. 13 lines 47-56).

Regarding claim 12, Toda further discloses constituent elements of the respective circuits are integrally formed on a semiconductor substrate (col. 1 line 55 through col. 2 line 7).

Regarding claim 13, Toda further discloses constituent elements of the respective circuits are integrally formed on a same semiconductor substrate with a CMOS process (col. 1 line 55 through col. 2 line 7).

***Conclusion***

5. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

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Facsimile responses should be faxed to:

(571) 273-8300

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Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571)272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis Kuntz can be reached on (571)272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Nguyen

Examiner

Art Unit 2643

CURTIS KUNTZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600